CROSS-REFERENCE TO RELATED APPLICATION

The following co-pending and co-assigned application contains related information and is hereby incorporated by reference:

Serial No. 09/590,506 (Attorney Docket No. 1043-EP [2836-P099US]), entitled "SYSTEM ON A CHIP", filed June 9, 2000, currently pending;

Serial No. 09/590,596 (Attorney Docket No. 1044-EP [2836-P102US]), entitled "CLOCK GENERATOR CIRCUITRY", filed June 9, 2000, currently pending; and

Serial No. 09/951,124 (Attorney Docket No. 1039-EP [2836-P104US]), entitled "VOLTAGE LEVEL SHIFTER", filed June 9, 2000, currently pending.

Attachment A shows all the changes relative to the previous version with text additions underlined, and text deletions bracket.

IN THE DETAILED DESCRIPTION

Please delete pages 70, 91 and 93 and substitute the following replacement pages 70, 91 and 93. Attachment A shows all the changes relative to the previous version with text additions underlined, and text deletions bracket.

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alternate system boot routine and support specialized testing by automatic test equipment. Among these specialized tests, are tests of the oscillator and PLLs, tests by test interface controller (TIC) of system internal functions through high speed bus 102, scan testing using Automatic Test Pattern Generation, observation testing which allows internal signals to be monitored through the Row and Column pins to keyboard interface 118, drive all float, drive all high and drive all low tests which cause all output capable pins to enter either a floating, logic high or logic low state, and a XOR tree test allowing all input capable pins to be connected to an XOR tree.

System 100 includes two phase-locked loops (PLLs) 131 which generate the clocks and similar timing signals necessary during device operation. PLLs 131 are configured with registers within system control clock 130. Among other things the multiply rate, the value which determines the number by which the reference clock is multiplied to produce the PLL output clock, is independently set for each PLL. Additionally, the output clock can be sent to an output pin for observation or a given PLL can be bypassed completely such that the output clock becomes the reference clock.

For a more complete description of the preferred clock generation circuitry used in system 100, reference is now made to copending, coassigned patent application Serial Number 09/590,596 (Attorney Docket Number 1044-EP [2836-P102US]).

IDE interface 132 operates from high speed bus 102 and supports ATAPI compliant connections to both external master and slave IDE devices, up to PIO Mode 4, Multiword DMA Mode

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Number) is input at Step 1738. Then, at Steps 1739 and 1740, the invalid flag is set and the sign bit is set to zero. The procedure next jumps to Step 1724 where the mantissa and exponent are concatenated with the new sign.

For a floating point negate operation, at Step 1724, the signaling NaN is input at Step 1742. The invalid flag is set at Step 1743 and the sign bit is inverted at Step 1744. This procedure then also jumps to Step 1724.

To convert an integer to a floating point value at Step 1745, a determination is first made as to whether the operand is a 32-bit or 64-bit integer (Step 1746). In the case of a 32-bit integer, the operand is sign extended at Step 1747 to 64 bits. The initial biased exponent is set at Step 1748 to 1084. At Step 1749 the first operand (Op1) presented to the adder is taken as the 64-bit value and the second adder operand (Opt2) is taken as zero. The procedure jumps to Step 1710 and these two operands are added as was described above for the floating point addition operation.

At Step 1751, the execution of the double precision to single precision operation is illustrated. First a determination is made as to whether the mantissa is too large or too small, and if so the corresponding flag is set (Step 1752). The input operand is rounded at Step 1752 to single precision. The process again jumps to Step 1724.

Finally, if at Step 1751 the decoded instruction does not invoke s double to single precision conversion, then at Step 1754 a value of 896 is added to the exponent and at Mode

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compliment multiplier array 1603. Fixed point adder 1604 then adds the sum and the carry bits from multiplier array 1603 and the contents of register Ppart at Step 1813.

In the preferred instruction set, provided herein as Appendix B, additional operations can be performed on 32-bit operands during the same instructions cycle. Among the instructions provided are 32-bit integer multiply-add, 32-bit integer multiply-subtract, 32-bit integer multiply-add, result to accumulator, 32-bit integer multiply-subtract, result to accumulator, 32-bit integer multiply-add to accumulator, and 32-bit integer multiply-subtract from accumulator instructions. These operations are represented in FIGURE 18 by Steps 1814-1817.

At Steps 1814 and 1815, a 32-bit addition or subtraction takes place. The source for the add in register can be one of the accumulators 1610 (FIGURE 16), or one of the C or B source registers. For instructions requiring storage in the accumulator at Step 1816, the accumulation takes place at 1817. Thereafter, the procedure can jump to Steps 1807-1809 where the result can be selectively shifted, and /or saturated and rounded and then forwarded to the register file or to another functional unit within the math coprocessor.

In the case of a 64-bit integer multiplication at Step 1810, the register Ppart is loaded with zero's (Step 1818). At Step 1819, the unsigned lower 32-bits of the X- and Y-integers are multiplied in the multiplier array and then the result of Psum1, Pcarry1 are added with the contents of Ppart at Step 1820. Next, the output of adder 1604 is